

REMARKS

In the above-identified Office Action, the Examiner has rejected claims 7-10 and 14 as being anticipated by the patent to Iida et al. Applicant has canceled claims 7, 8, 10 and 14 as above. Claim 9 is now of current concern. The Examiner has stated that the G_e/G_c ratio can be determined to be 1.16 and that an OSF region occupying a crystal diameter ratio of greater than 0.5 and less than $1.06 \times (G1_{center} \times G2_{center})^{-0.2}$ in Figure 10A. Applicant disagrees with the Examiner's conclusions in this regard.

The feature of the subject invention resides in that the silicon ingot is pulled up by controlling the temperature gradient to satisfy the conditions 1 and 2 of claim 9. Iida et al. does not describe such features at all.

Iida et al. describes in column 14, lines 39-45, with respect to the conditions for manufacturing the ingot shown in Figure 10A, that "The temperature gradient in an in-crystal descending temperature zone between a melting point of silicon and 1400°C in the vicinity of the solid-liquid interface was set as follows: $G_e = 45.0$ (°C/cm); $G_c = 42.0$ (°C/cm); $\Delta G = G_e - G_c = 3.0$ (°C/cm) ..."

When $G1_{edge}/G1_{center}$ of the condition 1 of claim 9 is calculated by using these values, $G_e/G_c = 1.07$ is obtained. This numeral 1.07 is completely out of range of the condition 1 of claim 9. Therefore, it is apparent that the ingot shown in Figure 10A of Iida et al. is not and cannot be manufactured by the method of claim 9.

There is no suggestion relative to the condition 2 of claim 9 that is taught or suggested from Figure 8 of Iida et al.

The Examiner apparently selected data from separate embodiments (Figure 8, Figure 10A) described in the specification of Iida et al. and applied them to the conditions 1 and 2 of claim 9 without any suggestion that such parameters are combinable. As a result, one skilled in the art would not find Iida et al. relevant or material to the technique of claim 9.

In addition to the above, the invention of claim 9 employs the parameters " $G1_{edge}/G1_{center}$ " and " $G1_{center} \times G2_{center}$ " and controls them, whereas Iida et al. is silent about the parameters " $G1_{edge}/G1_{center}$ " and " $G1_{center} \times G2_{center}$ " and the control of these parameters.

Furthermore, as described in column 2, lines 66 through column 3, line 6 of Iida et al., the

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technique of Iida et al. relates to wafers that have neither a V-rich region nor an I-rich region, i.e., defect-free wafers. As such, the target of the present invention differs from that of Iida et al. Therefore, the manufacturing method of the present invention cannot be taught or suggested by Iida et al.

Applicant hereby requests reconsideration and re-examination thereof.

With the above amendments and the remarks, this application is considered ready for allowance, and Applicants earnestly solicit an early notice of same. If the Examiner believes that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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